

# Event Plus Delay

*Poor man's version*

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The RETDAT protocol supports requests that specify replies to be returned on a clock event, but it does not support clock event plus delay, where one can ask the front end to delay some time before collecting the data. This note describes a "poor man's version" for such support that may require only minimal changes to RETDAT in the front ends and perhaps no changes to the client side.

The idea is suitable especially for such requests where the units of delay are 15 Hz cycles. For access to BLM waveform data, say, that is measured on the second 0x1D cycle in a series of consecutive 0x1D event cycles, this support may be "just the thing."

The `ftd` format for clock event specification is `0x80xx`, where the `xx` is the 8-bit clock event number. Assuming that the other 7 bits are not used for something else, they could be used to specify a delay in units of 15 Hz. In the IRM/PowerPC systems, asking for data to be returned on an event means it is returned at the normal 15 Hz time that everything else is returned, but only if the given event occurred within that last 66 ms. So, in these systems, talking about an event plus delay makes sense if the delay is in units of 15 Hz cycles.

An example of a need for which this suggestion might be a solution, consider the operation of multiple 15 Hz cycles of some particular event, such as 0x1D, which announces MiniBooNE cycles. If one wanted to capture data to be returned on the second of such cycles, this method could be used by specifying the event and a count of 1, meaning that data would be returned on the cycle following a 0x1D event. This simple logic would not reject data return on the cycle following a 0x1D cycle that was not also a 0x1D cycle, however. One could define another option that would act in this way: return data on the  $n^{\text{th}}$  consecutive cycle of 0x1D events, in which case a lone 0x1D event would not cause data to be returned. To specify another option, we might want to give up bit 14 of the `ftd`. If bit 15 and bit 14 were both set, it could mean this latter case; otherwise, the remaining 6-bit count could specify a number of cycles delay, for a maximum delay  $> 4$  seconds.