

# Digital Control Pulse Pair

*Variation of theme*

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Digital control types supported by the system code are of several kinds, including simple hi/lo control (dc) as well as single or dual pulse control. This note describes a new variation for the dual pulse control case.

The dual pulse control case allows for indicating a target Bit# via the Digital Control field in the Analog Descriptor (ADESC) table entry. Either that Bit# or the adjacent one can be pulsed, according to the state indicator specified. (The adjacent bit is defined as the Bit# gotten from the indicated one by toggling the least bit of the Bit#.) The dual control types supported until now assume that the direction of the formed pulse is the same for either of the pair of control bits. The new variation described here supports the case where the adjacent bit is controlled with the opposite polarity from that of target bit.

Take an example. Suppose we use dctype 6 to target Bit# 0103. The adjacent Bit# is 0102. There are two choices for control, generally referred to as "left" / "right." If the "left" choice is used, the indicated Bit# 0103 is pulsed; if the "right" choice is used, the adjacent Bit# 0102 is pulsed. In either case, the pulse is upward-going; the control line is set hi to initiate the pulse, then set lo some time later to complete the pulse.

In this example, if dctype 7 were used instead, the behavior would be the same, except that the pulse formed for either control line would be downward-going; the control line would be set lo to initiate the pulse, then set hi to complete it.

The new variation uses dctypes 8 and 9 to indicate that when the adjacent Bit# is targeted, because the "right" choice is selected, the pulse direction is also reversed. Again, in the above example, if the new dctype 8 is used, the pulse action will be upward-going for Bit# 0103, but it would be downward-going for adjacent Bit# 0102. Using the new dctype 9, the pulse direction would be downward for Bit# 0103, but upward for Bit# 0102.

Because it is possible to have external hardware automatically form the pulse, we also need another pair of dctypes to indicate that case. So for the new dctypes 8 and 9, the related hardware variations are dctypes 10 and 11. Here is the complete dctype table:

<i>Dctype#</i>	<i>Flavor</i>	<i>Action</i>
0	-	None. no digital control at all.
1	dc	Toggle to opposite state
2	dc	Set hi
3	dc	Set lo
4	p1	Pulse hi
5	p1	Pulse lo
6	p2	Pulse hi one of two adjacent bits
7	p2	Pulse lo one of two adjacent bits
8	p2	Pulse hi if indicated bit, pulse lo if adjacent bit
9	p2	Pulse lo if indicated bit, pulse hi if adjacent bit
10	p2	Hardware case of 8
11	p2	Hardware case of 9
12	p1	Hardware case of 4
13	p1	Hardware case of 5
14	p2	Hardware case of 6
15	p2	Hardware case of 7

To complete the picture of pulse-forming dctype, dctype 14 and 15 are the hardware variations for dctype 6 and 7. Also, dctype 12 and 13 are the hardware variations for dctype 4 and 5, for which there is only a single Bit# involved, and “left/right” has no significance. Dctype 4 forms an up-going pulse; dctype 5 forms a down-going pulse.

The significance of dctype 2 and 3 is to simply set the control line hi or lo, respectively. Dctype 1 indicates that the current control line is to be toggled, or switched to the opposite state. Dctype 0 indicates no digital control applies at all.

Note that for any pulse type, either p1 or p2, a delay is also specified. In the `ADESC` entry, only 4 bits are available for the dctype value and 4 bits are available for the delay, which is in units of operating cycles, such as 15 Hz. A value of zero for the delay results in a pulse of nominal width 20 microseconds.

The original document describing digital control types is called *Digital Control Pulses*.

Detailed changes for adding this option were made in modules `SetDC`, `SRMReq`, and `PLCQ`.