

Preliminary

Digital PMC Module for IRM-2400

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Introduction

The DigPMC card is a commercially available, general purpose, programmable PMC module that is configured to perform the digital interface tasks required by the Internet Rack Monitor, IRM, software. These tasks include TClk decoding, delay timers, and processing various digital I/O signals. The PMC module was a design developed jointly between Fermilab and Technobox Inc. In operation the module uses one of the two PMC sockets on the Motorola MVME-2400 PowerPC single board computer.

Technobox 2372 PMC

The Technobox 2372 is a PMC module that contains the following components:

- Altera 10k70 programmable logic array
- 128kBytes of static RAM
- Receivers for TClk and MDAT
- Programmable phase locked loop, PLL, clock generator
- 96 bits of digital I/O

When configured as the DigPMC, this module provides 32 bits of digital I/O accessible via the 68-pin front panel connector, organized as 4 bytes of data connected to I/O pins of the Altera chip using byte wide '245 style bidirectional buffers. The pinout of this connector is given in Figure 1. The Altera 10k70 may be programmed either by an onboard PROM at Reset time, or by downloading the program data over the network.

Functions of the DigPMC

The DigPMC makes use of the 32 bits of Digital I/O connected to the 68-pin front panel connector, and the TClk and MDAT input signals. TClk is decoded to find the 8-bit TClk events and the event numbers along with a microsecond resolution time stamp are stored in a 48-bit FIFO. Interrupts are generated as incoming TClk events are decoded. Eight delay timers are included, and the trigger output of Timer 0 causes an interrupt to the host processor. This interrupt is typically used to cause 15 Hz data acquisition to be started for each cycle. A byte of switch input and a byte of output LEDs are also included. Two Relay outputs are available for use as 'beam inhibit' contacts activated by the host processor.

TimeStamp

A 32-bit TimeStamp counter is included in the Altera FPGA. This is a free running counter that is incremented by a 1 MHz pulse train derived from the decoded TClk signal. In the absence of a TClk signal, the output of the PMC's onboard Phase locked loop frequency generator is used. The instantaneous value of the counter may be read by the host computer at any time, and the value of the counter is stored in the event FIFO along with TClk event values each time an event is detected. An interrupt is generated whenever the FIFO output Ready is asserted. This allows the host computer to keep a current map of detected clock events and their arrival time.

TClk processing

With the aid of the clock receiver circuitry and a solid state tapped delay line, TClk events are decoded and the value of each event is recorded in a 48-bit x 256-word FIFO memory, along with the current value of a 32-bit time stamp counter. The timestamp counter is a free-running counter that is incremented at 1 Mhz signal which is derived from the decoded 10 MHz TClk frequency. In the absence of an input TClk signal, the timestamp counter input signal is derived from the onboard 20 MHz PLL Clock. The FIFO Output Ready signal causes an interrupt for the host computer.

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Delay Timers

The 8-channel delay timer has the characteristics of a “177” style timer. That is, 8 independent delay timers that can each be triggered by the occurrence of one or more TClk events. Each timer has associated with it, a 16-bit delay, a 16-bit output pulse width and a control register. The memory map given in Figure 2 shows the memory locations of the individual timer delay and pulse width and control register parameters, and also gives the locations of other global parameters for the DigPMC module. The definition of bits in the control registers are detailed in Figure 3.

DigPMC Access Module

In operation, the DigPMC is used in conjunction with a DigPMC Access module shown in Figure 4. This module connects to the 68-pin connector of the DigPMC to provide a way to access signals in that connector. The Access module has a byte of sense switches, twelve diagnostic LEDs, and a 20-pin diagnostic Berg connector that provides test points that can be viewed on oscilloscopes and logic analyzers. The pinout of this 20 pin diagnostic connector is included in Figure 1. An internal ribbon cable from the Access module to a companion Timer Fanout module allows for connectorized access to the eight channel delay timer (Figure 5). A TClk input and Timer 2 out Lemo connectors are provided so that TClk can be connected to the DigPMC module in case a Timer Fanout board is not used. All eight timer outputs are available on P2 at the rear of the module. The pin locations are given in Figure 6.

Twelve LED indicators are located on the front panel of the DigPMC Access module. Four of these are permanently assigned to FIFO Output Ready, IRQ, Relay-0, and Relay-1 as shown in Figure 4. The other eight LEDs are assigned to one of two groups, TaskLEDs and MiscLEDs. Each of the four TaskLEDs can be assigned to indicate the state of a single bit of a 16-bit task LED word. The assignment is made for each LED by a 4-bit value stored in the TaskLED Mux Select [3..0] register. Similarly using the MiscLED Mux Select register, each of the four MiscLEDs can be programmed to show the state of a bit in the 16-bit MiscLED Register. This arrangement provides a programmable way of showing four of the bits of a 16-bit word for both the Task and Misc LED registers. Bit assignments for the TaskLED and MiscLED Mux Select registers are given in Figures 7a and 7b, respectively. These LEDs are used for software diagnostics and timing.

Access to several test signals is provided by a 20-pin Berg connector on the front panel of the DigPMC Access Module. Pin assignments for these signals is included in Figures 1 and 4.

Signal	JI Conn#	20 Pin Hdr
TClk In	1	
Delay-0	2	
Delay-1	3	
Delay-2	4	
Delay-3	5	
Delay-4	6	
Delay-5	7	
Delay-6	8	
Delay-7	9	
Tclk Out	10	17
Tclk Out	11	15
10 MHz Out	12	13
1 MHz Out	13	11
FIFO Output Ready	14	3
IRQ	15	5
Relay-0	16	7
Event \$AF	17	9
Gnd	35..68	1, 19

Note: Pins J1-35..J1-68 are Gnd.

Signal	JI Conn#	20 Pin Hdr
Sw-0	18	
Sw-1	19	
Sw-2	20	
Sw-3	21	
Sw-4	22	
Sw-5	23	
Sw-6	24	
Sw-7	25	
LED-0	26	4
LED-1	27	6
LED-2	28	8
LED-3	29	10
LED-4	30	12
LED-5	31	14
LED-6	32	16
LED-7	33	18
MDAT In	34	
Gnd		2, 20

Figure 1. Digital PMC Pinout

	0 / 8	2 / A	4, C	6, E
Base + \$00	Delay 0	Width 0	Control Reg 0	S/W Trigger Timer0
Base + \$08	Delay 1	Width 1	Control Reg 1	S/W Trigger Timer1
Base + \$10	Delay 2	Width 2	Control Reg 2	S/W Trigger Timer2
Base + \$18	Delay 3	Width 3	Control Reg 3	S/W Trigger Timer3
Base + \$20	Delay 4	Width 4	Control Reg 4	S/W Trigger Timer4
Base + \$28	Delay 5	Width 5	Control Reg 5	S/W Trigger Timer5
Base + \$30	Delay 6	Width 6	Control Reg 6	S/W Trigger Timer6
Base + \$38	Delay 7	Width 7	Control Reg 7	S/W Trigger Timer7
Base + \$40	Del 0 Ctr	Width 0 Ctr	Del 1 Ctr	Width 1 Ctr
Base + \$48	Del 2 Ctr	Width 2 Ctr	Del 3 Ctr	Width 3 Ctr
Base + \$50	Del 4 Ctr	Width 4 Ctr	Del 5 Ctr	Width 5 Ctr
Base + \$58	Del 6 Ctr	Width 6 Ctr	Del 7 Ctr	Width 7 Ctr
Base + \$60	Master Contrl Reg	---- • Switches	---- • Relay1	---- • Relay0
Base + \$68	---- • Prescale Sync Event	---- • ----	Interrupt Mask	Interrupt Status
Base + \$70	MiscLED Mux[7..4]	TaskLED Mux[3..0]	Misc LED Reg	Task LED Reg
Base + \$78	FIFO Timestamp High	FIFO Timestamp Low	---- • Event FIFO	FIFO Out Rdy•TCLK Stat
Base + \$80	Count1MHzHigh	Count1MHzLow	Count 2KHz	
Base + \$88				
Base + \$100	Start of Trigger RAM	----	----	----
----	----	----	----	----
Base + \$1FF	----	----	----	End of Trigger RAM

Base + \$65 lsb is used for Relay 1
Base + #67 lsb is used for Relay 0
Base + \$7E: msb is FIFO Output Ready
Base + \$7F: lsb is TCLK Status
Base + \$100...Base + \$1FF; Trigger RAM.

Figure 2. Memory Map for Digital Board

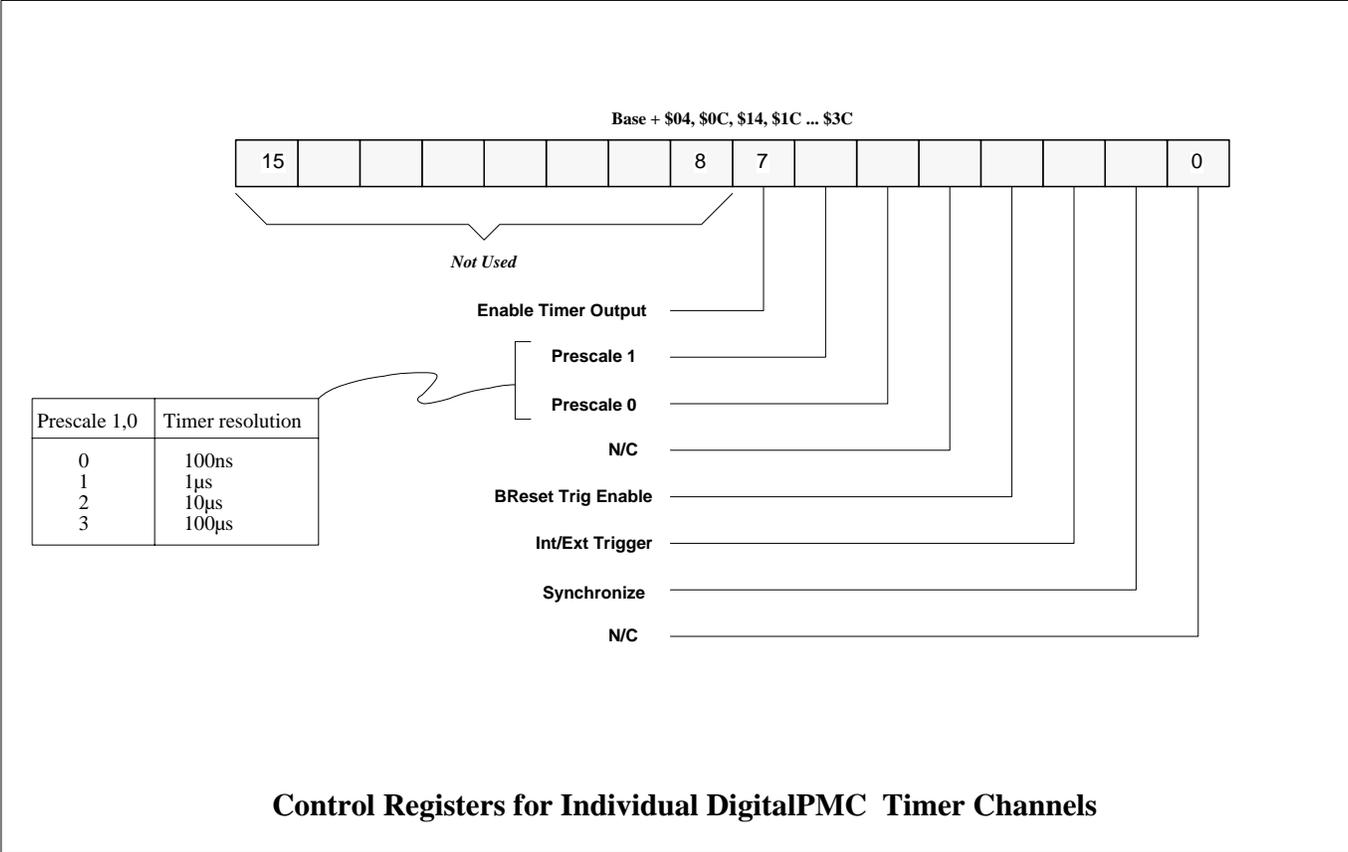
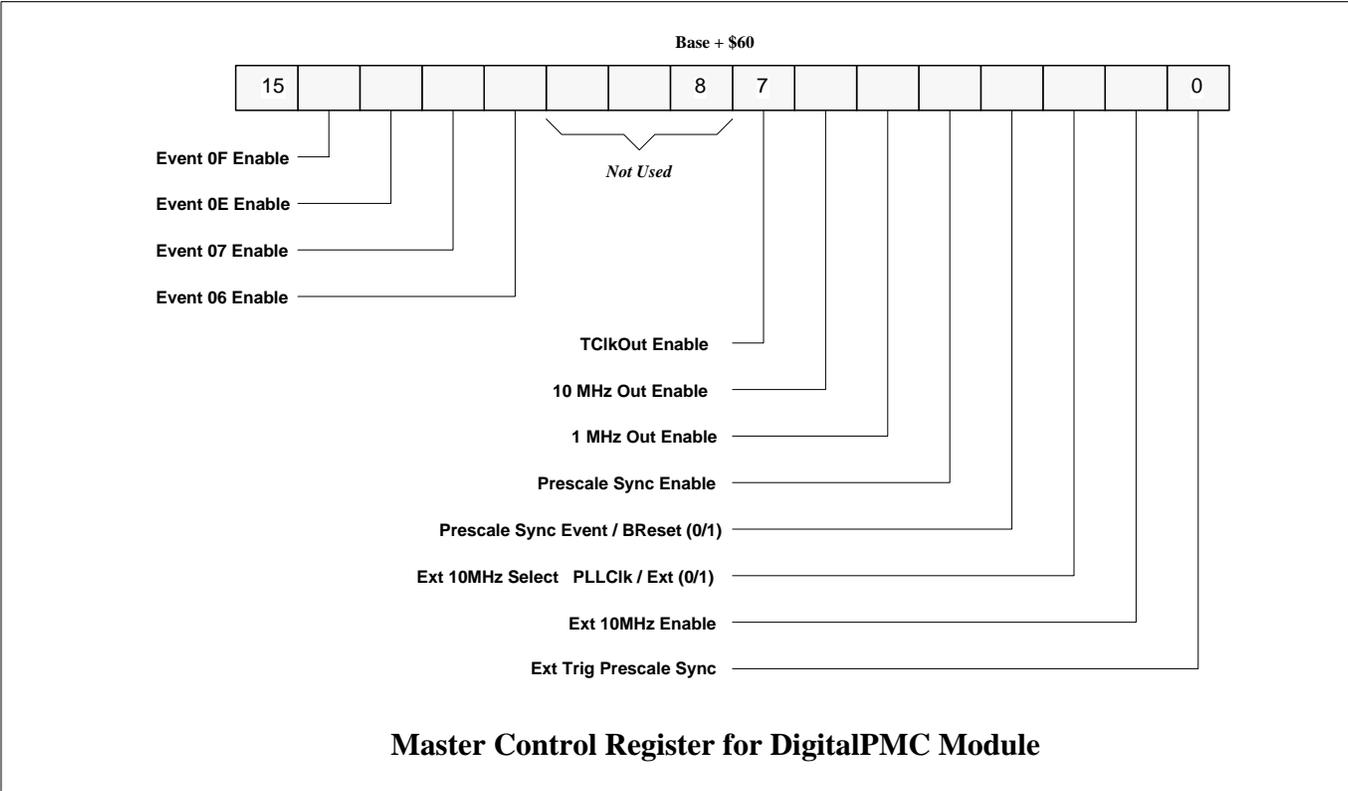


Figure 3.

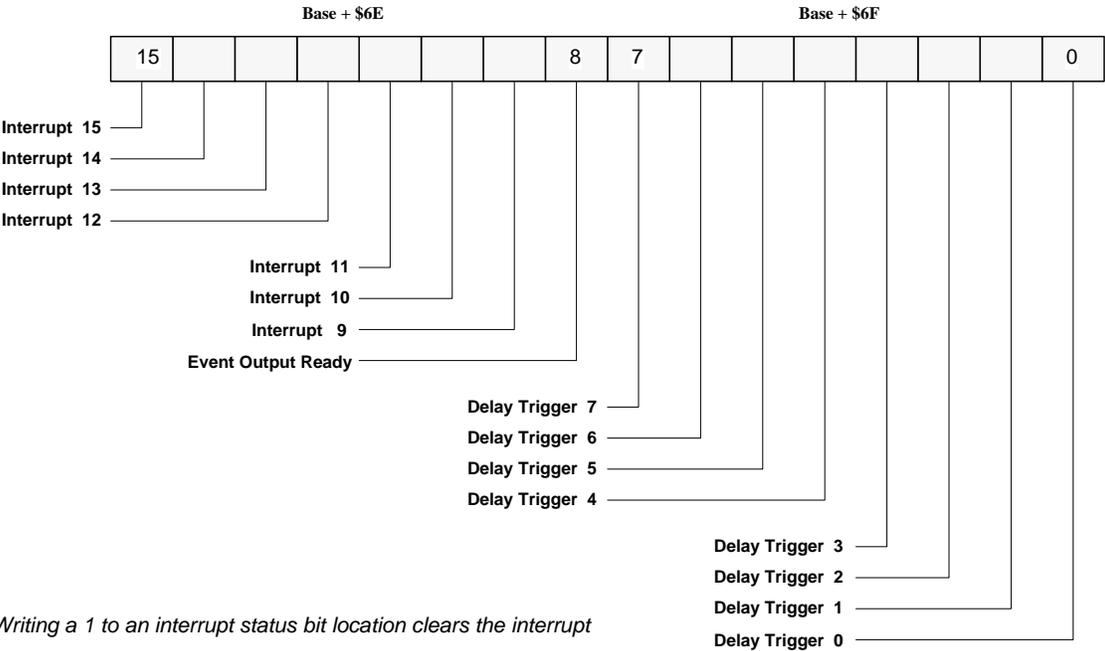


Figure 8a. DigPMC Module Interrupt Status Register

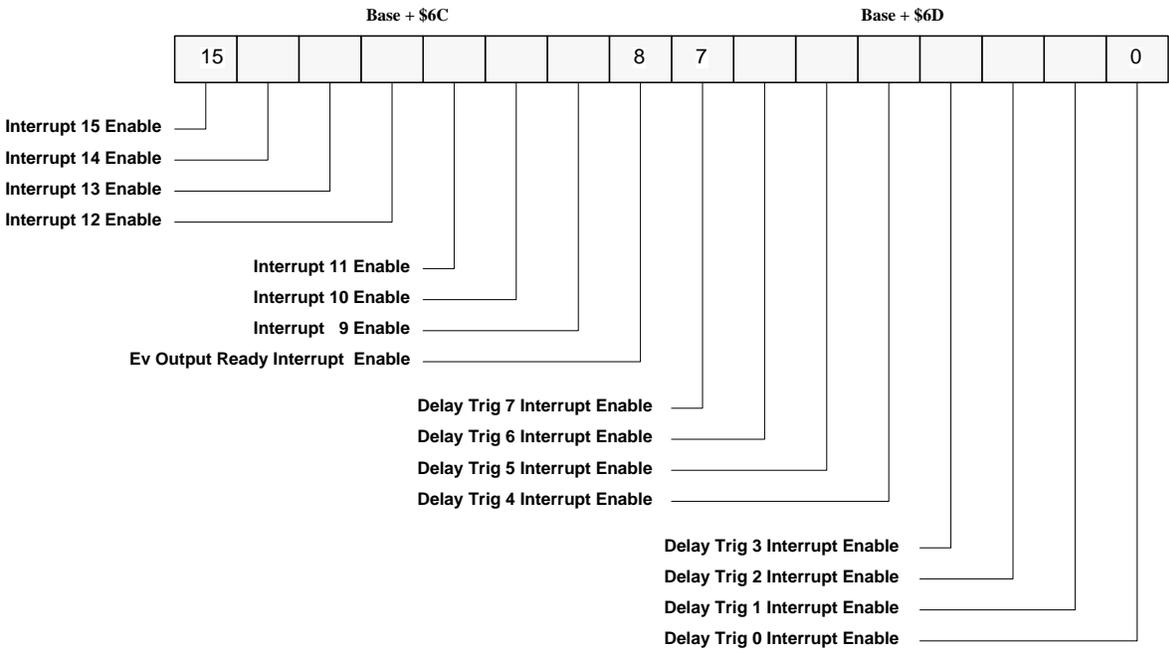


Figure 8b. DigPMC Module Interrupt Mask Register

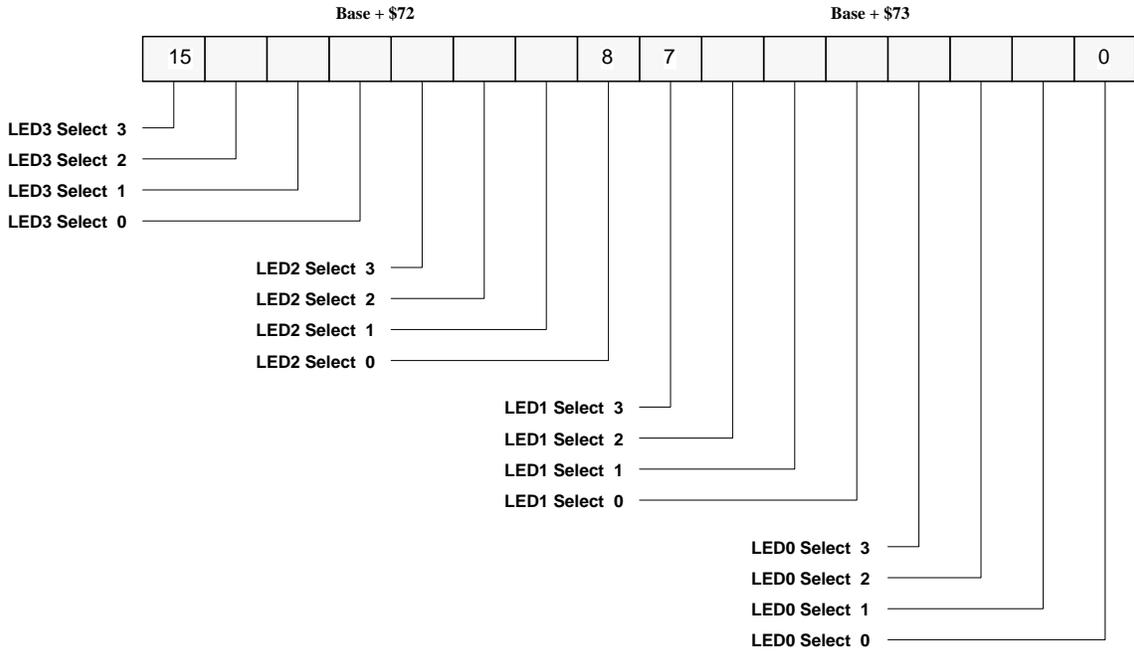


Figure 7a. DigPMC LED [3..0] Mux Select (TaskLED Select)

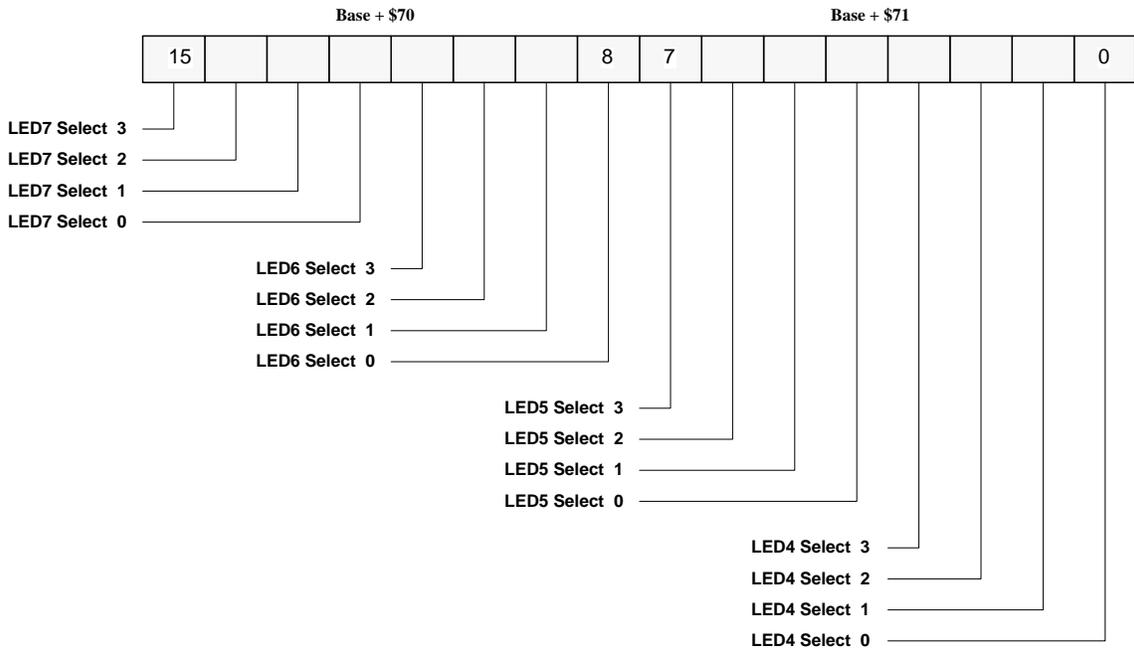


Figure 7b. DigPMC Module LED [7..4] Mux Select (MiscLED Select)

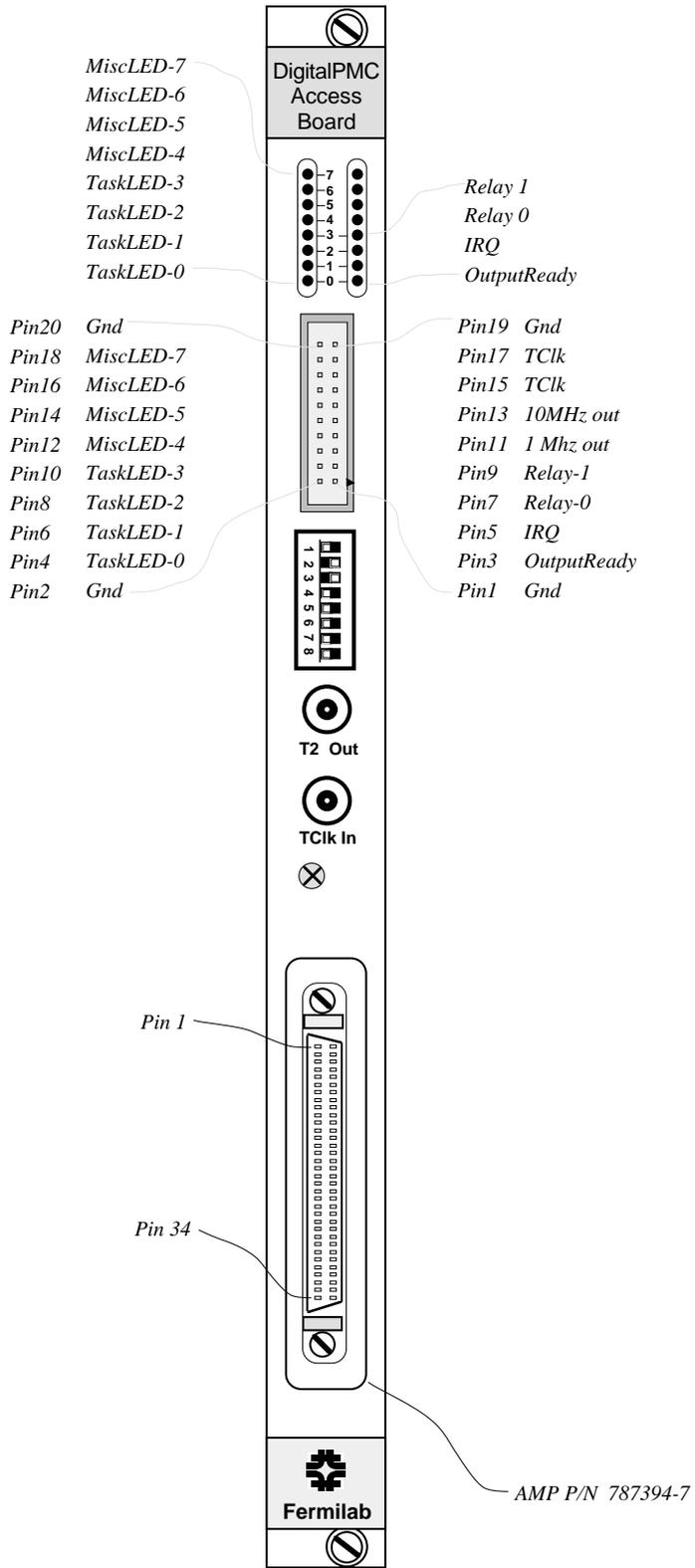


Figure 4. DigPMC Access module

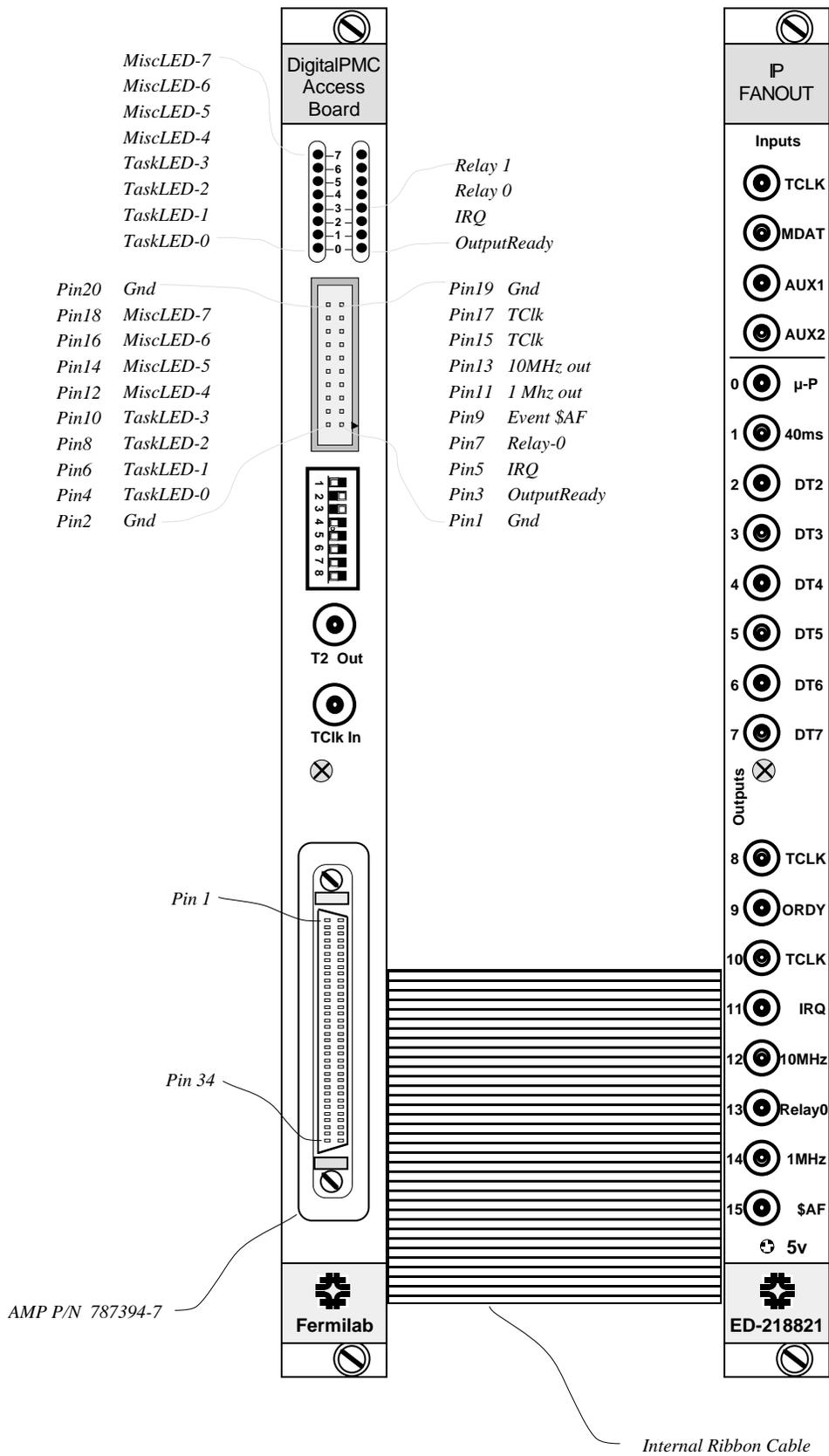


Figure 5. DigPMC Access module with Timer Fanout

Signal	Row C	Row A	Signal
Relay1c	C32	A32	Relay1cr
Relay2c	C31	A31	Relay2cr
ExtTrig	C30	A30	Gnd
ExtClk	C29	A29	Gnd
–	C28	A28	Gnd
–	C27	A27	Gnd
TclkOut	C26	A26	Gnd
–	C25	A25	Gnd
Delay1	C24	A24	Gnd
Delay2	C23	A23	Gnd
Delay3	C22	A22	Gnd
Delay4	C2	A21	Gnd
Delay5	C20	A20	Gnd
Delay6	C19	A19	Gnd
Delay7	C18	A18	Gnd
–	C17	A17	Gnd
–	C16	A16	Gnd
–	C15	A15	Gnd
–	C14	A14	Gnd
–	C13	A13	Gnd
–	C12	A12	Gnd
–	C11	A11	Gnd
–	C10	A10	Gnd
–	C9	A9	Gnd
–	C8	A8	Gnd
–	C7	A7	Gnd
–	C6	A6	Gnd
–	C5	A5	Gnd
–	C4	A4	Gnd
–	C3	A3	Gnd
–	C2	A2	Gnd
–	C1	A1	Gnd

Figure 6. DigPMC Access Card VMEbus P2 Connector Pinout